REMARKS

Claims 1-2, 6-12, and 33-40 are pending in the application, claims 3-5 and 13-32 having been withdrawn from consideration as being directed to unelected inventions. The Examiner rejected claims 1-2, 6-12, and 33-40 under 35 U.S.C. §103(a). By this amendment, Applicant has canceled without prejudice unelected claims 3-5 and 13-32. Applicant reserves the right to further prosecute these claims in a continuing or divisional application.

Section 103 Rejections

Claims 1, 7-9, and 11-12 were rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,920,084 (Gu, *et al.*) in view of U.S. Patent No. 5,053,844 (Murakami, *et al.*).

Claims 33, 37, and 39-40 were rejected under 35 U.S.C. §103(a) as being obvious over Gu in view of U.S. Patent No. 5,646,756 (Dohjo, *et al.*).

Claims 2 and 34-36 were rejected under 35 U.S.C. §103(a) as being obvious over Gu, Murakami and Dohjo.

Claims 10 and 38 were rejected under 35 U.S.C. §103(a) as being obvious over Gu, Murakami and Dohjo, and further in view of U.S. Patent No. 5,671,027 (Sasano, *et al.*).

Applicant respectfully traverses this rejection.

Applicant's claim 1 is directed to a thin film transistor array substrate, and includes a "an insulating substrate; a first signal line formed on the insulating substrate; a first insulating layer formed on the first signal line; a second signal line formed on the first insulating layer while crossing over the first signal line; a thin film transistor connected to the first and the second signal lines; a second insulating layer formed on the thin film transistor, the second insulating layer having dielectric constant about 4.0 or less, the second insulating layer is formed with an a-Si:C:O layer or an a-Si:O:F layer and the second insulating layer having a first contact hole exposing a predetermined electrode of the thin film transistor; and

a first pixel electrode formed on the second insulating layer while being connected to the predetermined electrode of the thin film transistor through the first contact hole." This second insulating layer is used due to its dielectric constant for reducing parasitic capacitance between the between the first pixel electrode and the second signal line.

The Action concedes that Gu fails to disclose a second insulating layer formed with a a-Si:C:O layer or an a-Si:O:F, but then cites Murakami as disclosing an insulating a-Si layer formed from a-Si:O:F. However, Murakami is directed to an amorphous silicon photosensor, which is a technical field that is not analogous to that of a thin film transistor array panel. Murikami's photosensor includes three or four amorphous silicon layers. The materials used for Murikami's photosensor layers are chosen for specific bandgap properties to produce a sensor with a high Ip/Id ratio and applicable to sensing color. Murikami discloses the use of a-Si:O:F as a second end amorphous silicon layer, which has an optical band gap of 1.9 eV or more. Thus, the purpose of Murikami's amorphous silicon layer, adjusting a bandgap in a photosensor, does not teach or suggest that of Applicant's a-Si:O:F layer, reducing parasitic capacitance in a transistor circuit.

Thus, there is no suggestion or motivation in Murikami to use a "second insulating layer . . . formed with an a-Si:C:O layer or an a-Si:O:F layer" as claimed in Applicant's claim 1. In addition, there is no reasonable expectation that one successfully could combine the LCD disclosed in Gu with the photosensor of Murikami to produce the invention recited in Applicant's claim 1. Thus, Applicant urges that claim 1 is not *prima facie* obvious in view of Gu and Murakami. Reconsideration and withdraw of this rejection are respectfully requested.

Claims 2 and 7-12 depend from claim 1, and are thus patentable for at least the same reasons as claim 1. Reconsideration and withdraw of these rejections are respectfully requested.

Applicant's claim 33 is directed to a thin film transistor array substrate, and includes a "first insulating layer [that] includes a top layer and a bottom layer, the bottom layer having

dielectric constant about 4 or less, and the top layer being a silicon nitride layer."

The Action concedes that Gu fails to disclose a second dielectric layer having dielectric constant of about 4 or less, and then cites Dohjo (col. 7, lines 20-30) as disclosing an insulating layer with a top layer made of silicon nitride and a bottom layer made of low dielectric material, such as SiO_x, having a dielectric constant about 4 or less.

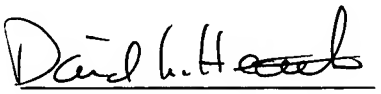
Applicant respectfully disagrees with this interpretation of Dohjo. The SiO_x material cited by the examiner is a material known by one skilled in the art as a material having a dielectric constant not about or less than 4.0. Thus, even if the teaching of Dohjo was consistent with Gu, there is no teaching or suggestion in Dohjo of an insulating layer including "a top layer and a bottom layer, the bottom layer having dielectric constant about 4 or less, and the top layer being a silicon nitride layer", as recited in Applicant's claim 33. Thus, Applicant urges that claim 33 is not *prima facie* obvious in view of Gu and Dohjo. Reconsideration and withdraw of this rejection are respectfully requested.

Claims 34-40 depend from claim 33, and are thus patentable for at least the same reasons as claim 33. Reconsideration and withdraw of these rejections are respectfully requested.

CONCLUSION

Applicant urges that claims 1-2, 7-12, and 33-40 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

By: 

David L. Heath
Reg. No. 46,763
Attorney for Applicant

Mailing Address:

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11767
(516) 692-8888
(516) 692-8889 (FAX)